

## 30V P-Ch Power MOSFET

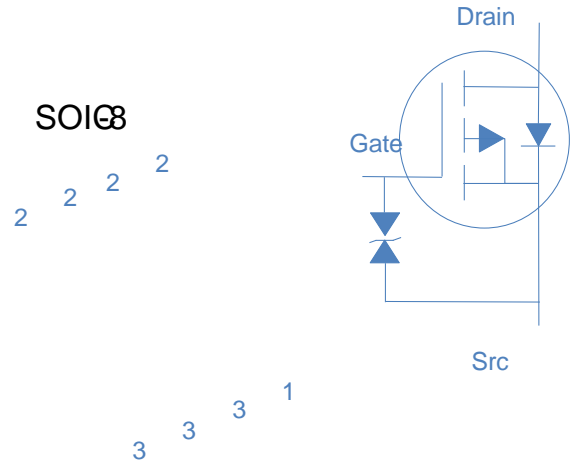
### Feature

- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested / 100% Rg Tested
- Lead Free, Halogen Free

$V_{DS}$		-30	V
$R_{DS(on),typ}$	$V_{GS}=10V$	7	m $\Omega$
$R_{DS(on),typ}$	$V_{GS}=4.5V$	12	m $\Omega$
$I_D$ (Silicon Limited)		-15	A

### Application

- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial



Part Number	Package	Marking
HTS085P03E	SOIC-8	TS085P03E

### Absolute Maximum Ratings at $T_j=25$ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	$I_D$	$T_C=25$	-15	A
		$T_C=100$	-11	
Drain to Source Voltage	$V_{DS}$	-	-30	V
Gate to Source Voltage	$V_{GS}$	-	$\pm 20$	V
Pulsed Drain Current	$I_{DM}$	-	-60	A
Avalanche Energy, Single Pulse	$E_{AS}$	$L=0.1mH, T_C=25$	31.25	mJ
Power Dissipation	$P_D$	$T_A=25$	2.5	W
Operating and Storage Temperature	$T_J, T_{stg}$	-	-55 to 150	

### Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	/W
Thermal Resistance Junction-Lead	$R_{\theta JL}$	25	/W

**Electrical Characteristics at  $T_j=25$  (unless otherwise specified)**
**Static Characteristics**

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-1.5	-3.0	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS}=0V, V_{DS}=-24V, T_j=25$	-	-	-1	$\mu A$
		$V_{GS}=0V, V_{DS}=-20V, T_j=125$	-	-	-10	
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	$\pm 10$	$\mu A$
Drain to Source on Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-12A$	-	7	8.5	m $\Omega$
		$V_{GS}=-4.5V, I_D=-9A$	-	12	15	
Transconductance	$g_{fs}$	$V_{DS}=-5V, I_D=-12A$	-	26	-	S
Gate Resistance	$R_G$	$V_{GS}=15mV, V_{DS}=0V, f=1MHz$	-	3.5	-	$\Omega$

**Dynamic Characteristics**

Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}=-15V, f=1MHz$	-	3091	-	pF
Output Capacitance	$C_{oss}$		-	476	-	
Reverse Transfer Capacitance	$C_{rss}$		-	404	-	
Total Gate Charge	$Q_g (10V)$	$V_{DD}=-15V, I_D=-10A, V_{GS}=-10V$	-	54	-	nC
	$Q_g (4.5V)$		-	32	-	
Gate to Source Charge	$Q_{gs}$		-	7	-	
Gate to Drain (Miller) Charge	$Q_{gd}$		-	13	-	
Turn on Delay Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-1A, V_{GS}=-10V, R_G=2.7\Omega,$	-	24	-	ns
Rise time	$t_r$		-	20	-	
Turn off Delay Time	$t_{d(off)}$		-	70	-	
Fall Time	$t_f$		-	12	-	

**Reverse Diode Characteristics**

Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_F=-3.6A$	-		-1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F=-3.6A, dI_F/dt=100A/\mu s$	-	52	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	60	-	nC

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage
Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature
Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

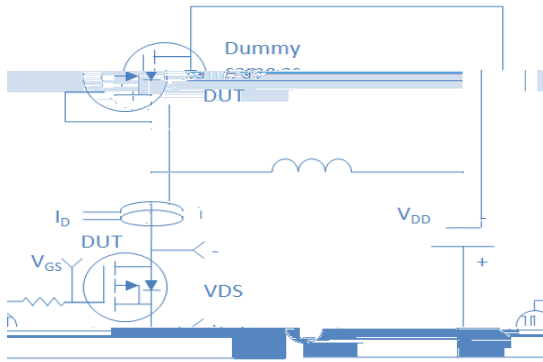


Figure 9. Maximum Safe Operating Area

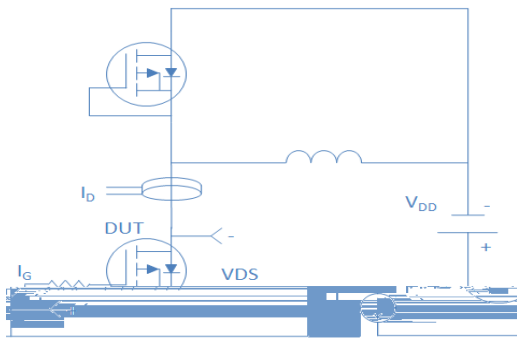
Figure 10. Single Pulse Maximum Dissipation

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

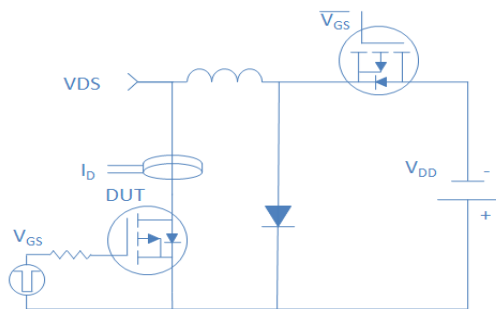
Inductive switching Test



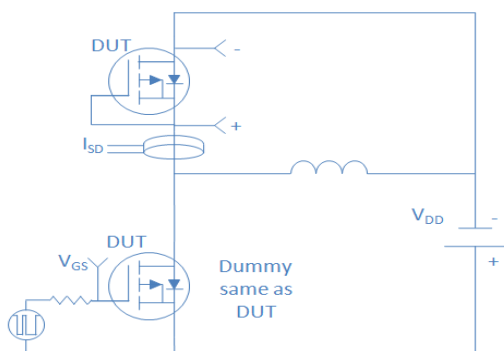
Gate Charge Test



Uclamped Inductive Switching (UIS) Test



Diode Recovery Test



Package Outline

SOIC-8, 8leads

